IDEC Chip Design Contest

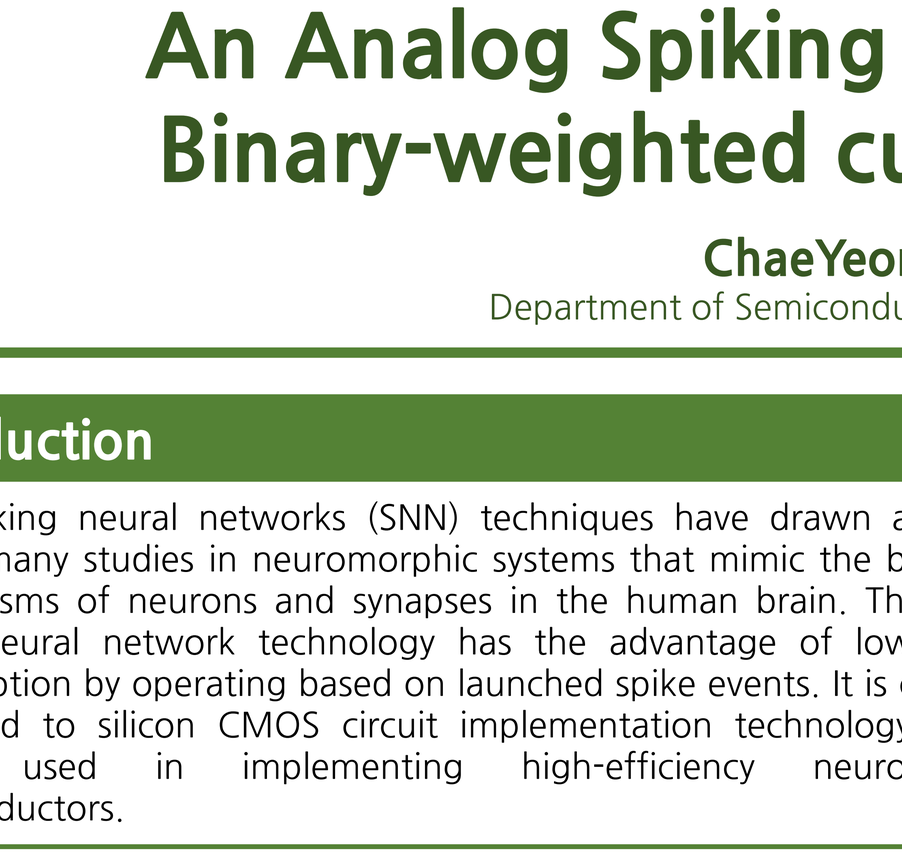
An Analog Spiking Neural Network Model with Binary-weighted current DAC and Comparator

ChaeYeon Shin and ByungDo Yang
Department of Semiconductor Engineering, Chungbuk National University

Introduction

The Spiking neural networks (SNN) techniques have drawn attention during many studies in neuromorphic systems that mimic the biological mechanisms of neurons and synapses in the human brain. The Spike-based neural network technology has the advantage of low power consumption by operating based on launched spike events. It is currently expanded to silicon CMOS circuit implementation technology and is widely used in implementing high-efficiency neuromorphic semiconductors.

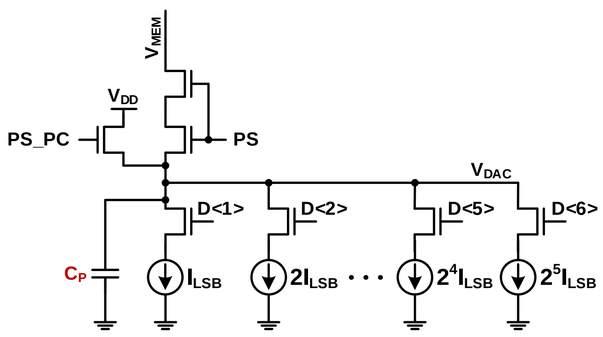
Architecture

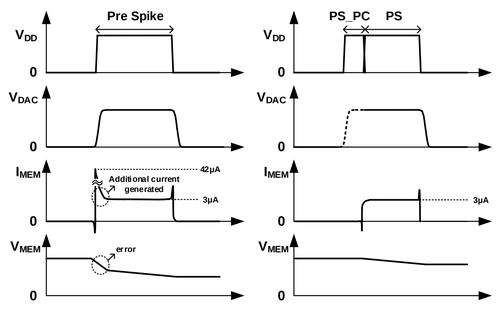


Proposed analog spiking neural network model

The model consists of N pre-spikes and M post-spikes. In each synapse, the V_{MEM} of the neuron is reduced with a current proportional to the weight, which is compared to the reference voltage.

Synapse circuit

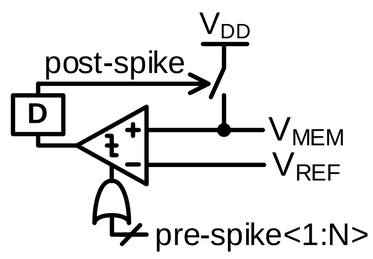


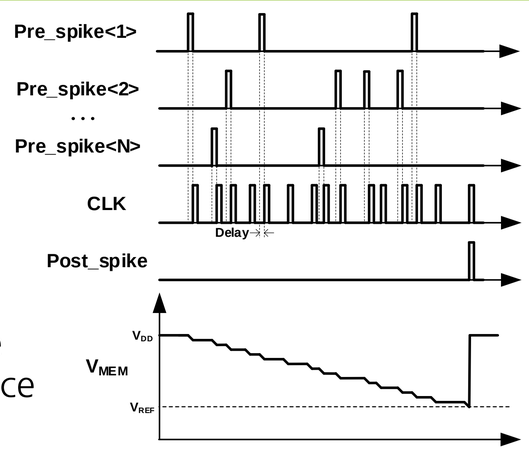


Proposed synapse circuit

The Synapse circuit receives pre-spikes from other neurons, generating currents proportional to the weights and reducing membrane voltages. It stores the weights as digital values to fine-tune the weights to implement circuits similar to the behavior of real synapses. The proposed synapse circuit improves area efficiency by replacing large capacitors used in existing synapses with binary-weighted current DAC. The parasitic capacitor that generates the error is reduced by adding a pre-charge switch.

Neuron circuit



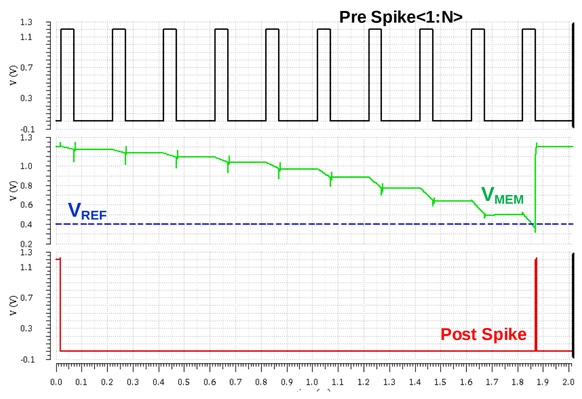


Proposed neuron circuit

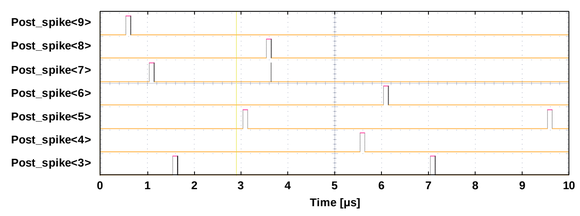
The neuron circuits compare membrane voltage with reference voltage to produce post-spikes.

Results

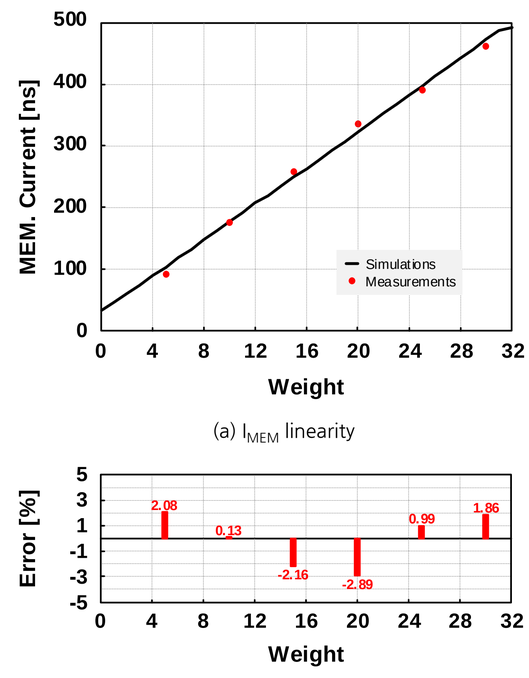
The measurement results of the implemented 6-bit DAC satisfy a resolution of 5 bits.



Simulation result



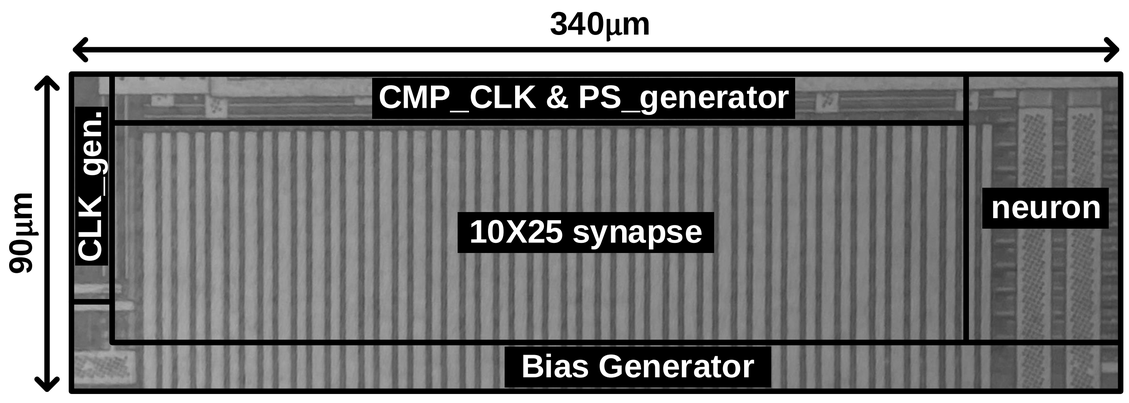
Measurement result



(a) I_{MEM} linearity

(b) Linearity error

Measurement Linearity



Chip layout & photograph

Conclusions

This chip proposes an analog SNN circuit using binary-weighted current DACs and comparators. The proposed synapse circuit achieves stable and high resolution and reduces the area by replacing a capacitor with binary-weighted current DAC. In addition, the proposed neuron circuit consists of a comparator that uses input signals as clocks instead of analog amplifiers, which can reduce power by up to 85%.

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

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